WHAT IS CLAIMED IS:

1. A method for processing data in a processor with an instruction, wherein the data is related to an array of elements, the method comprising steps of:

loading a first value from a first location;

loading a second value from a second location;

comparing the first and second values to each other;

optionally storing a predetermined value in a destination based upon the comparing step.

2. The method for processing data in the processor with the instruction, wherein the data is related to the array of elements as recited in claim 1, wherein:

the first location and second location are source registers, and

the destination is a destination register.

3. The method for processing data in the processor with the instruction, wherein the data is related to the array of elements as recited in claim 1, wherein the first and second values are operands.

4. The method for processing data in the processor with the instruction, wherein the data is related to the array of elements as recited in claim 1, wherein the predetermined value is zero.

5. The method for processing data in the processor with the instruction, wherein the data is related to the array of elements as recited in claim 1, wherein the comparing step comprises determining if the array index is greater than or equal to zero and less than a length of the array.

6. The method for processing data in the processor with the instruction, wherein the data is related to the array of elements as recited in claim 1, wherein the destination includes a base address for the array.

7. The method for processing data in the processor with the instruction, wherein the data is related to the array of elements as recited in claim 1, wherein the storing step further includes setting a flag.

8. The method for processing data in the processor with the instruction, wherein the data is related to the array of elements as recited in claim 1, wherein the first and second values are at least one of a signed integer and an unsigned integer.

9. The method for processing data in the processor with the instruction, wherein the data is related to the array of elements as recited in claim 1, wherein the first location comprises a length of the array.

10. The method for processing data in the processor with the instruction, wherein the data is related to the array of elements as recited in claim 1, wherein the second location includes an index of the array.

11. The method for processing data in the processor with the instruction, wherein the data is related to the array of elements as recited in claim 1, wherein:

the first location includes a length of the array

the second location includes an index of the array.

12. An instruction processor that operates upon a first source register having a first operand and a second source register having a second operand, comprising:

an operand compare function which compares the first and second operands;

decision logic coupled to the operand compare function which determines if the second operand is at least one of greater than zero and equal to zero; and

a flag setting function coupled to the decision logic.

13. The instruction processor that operates upon the first source register having the first operand and the second source register having the second operand of claim 12, wherein the flag setting function stores a zero in a destination register.

14. The instruction processor that operates upon the first source register having the first operand and the second source register having the second operand of claim 12, wherein the operand compare function loads the first and second operands respectively from a first and second source registers.

15. The instruction processor that operates upon the first source register having the first operand and the second source register having the second operand of claim 12, wherein the flag setting function is coupled to a destination register.

16. A method for processing an array by a processor, the method comprising the steps of:

determining if an array index is valid;

replacing a base address with a predetermined value based upon results from the determining if an array index is valid step; and

determining if a base address of the array is valid.

17. The method for processing the array by the processor of claim 16, further comprising the step of loading a first and second very long instruction words, where each includes a plurality of sub-instructions.

18. The method for processing the array by the processor of claim 17, wherein the first and second very long instruction words accomplish the determining steps and a step of loading an array element at an index address.

19. The method for processing the array by the processor of claim 16, wherein the predetermined value is an invalid base address.

20. The method for processing the array by the processor of claim 16, further including the step of calculating an address offset.

21. The method for processing the array by the processor of claim 16, further including the step of adding an address offset to the base address.

22. The method for processing the array by the processor of claim 16, wherein the predetermined value is zero.

23. The method for processing the array by the processor of claim 16, wherein the step of determining if array index is valid includes the steps of:

determining if the array index is with a range from zero to an array length minus one; and

determining if the array index is less than the array length.